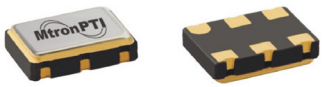
M630x Series

5x7 mm, 1.8/2.5/3.3 V, LVPECL/LVDS/CML/CMOS, TCXO/TCVCXO

QiK Chip™



RoHS Compliant

Features:

- TCXO/TCVCXO Featuring ***QiK Chip™*** Technology
- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 50 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

Applications:

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

Ordering Information

M6300	2	J	B	V	P	N	00.0000 MHz

Product Series
M6300 = 3.3 V
M6301 = 2.5 V
M6302 = 1.8 V

Temperature Range
1: 0 °C to +70 °C
2: -40 °C to +85 °C
3: -55 °C to +105 °C
4: -55 °C to +125 °C
6: -20 °C to +70 °C

Stability
G: ±0.5 ppm
H: ±2.5 ppm
J: ±1.0 ppm
L: ±4.6 ppm
K: ±2.0 ppm
E: ±10 ppm

Enable/Disable Function
B: Enable High (Pad 1)
S: Enable Low (Pad 1)
U: No Enable/Disable Function
G: Enable High (Pad 2)
M: Enable Low (Pad 2)

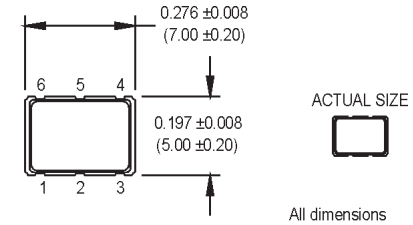
Output Type
F: No Voltage Control (TCXO)
V: Voltage Control (TCVCXO)

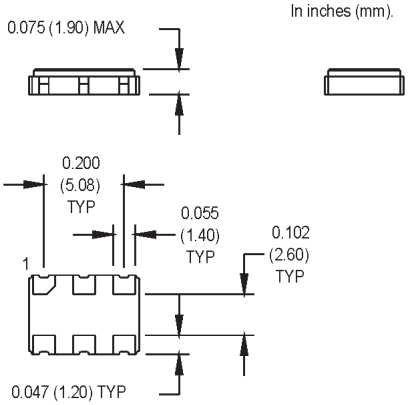
Output Waveform
P: LVPECL
L: LVDS
M: CML
C: CMOS

Package/Lead Configurations
N: Leadless Ceramic (9 Pad)
C: Leadless Ceramic (6 Pad)

Frequency (customer specified)

M6300Sxxx, M6301Sxxx & M6302Sxxx - Custom datasheets.





PIN 1 ENABLE

Pad 1: Enable/Disable
Pad 2: N/C
Pad 3: GND
Pad 4: Output Q (LVPECL, LVDS, CML, CMOS)
Pad 5: Output Q̄ (LVPECL, LVDS, CML)
Pad 6: V_{cc}

PIN 2 ENABLE

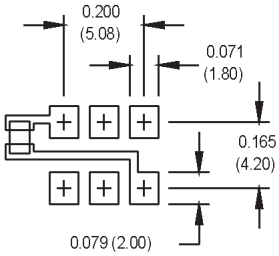
Pad 1: N/C, V Control
Pad 2: Enable/Disable
Pad 3: GND
Pad 4: Output Q (LVPECL, LVDS, CML, CMOS)
Pad 5: Output Q̄ (LVPECL, LVDS, CML)
Pad 6: V_{cc}

Temperature vs. Stability

	±0.5 ppm	±1.0 ppm	±2.0 ppm	±2.5 ppm	±4.6 ppm
0 °C to +70 °C	A	A	A	A	A
-20 °C to +70 °C	N	A	A	A	A
-40 °C to +85 °C	N	A	A	A	A
-55 °C to +105 °C	N	N	N	N	A
-55 °C to +125 °C	N	N	N	N	A

A = Available
N = Contact Factory

SUGGESTED SOLDER PAD LAYOUT



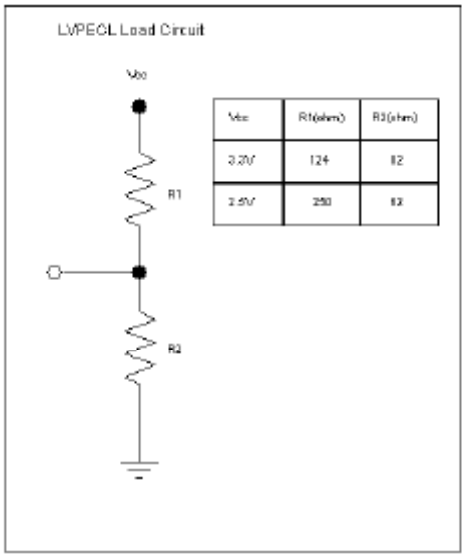
M630x Series

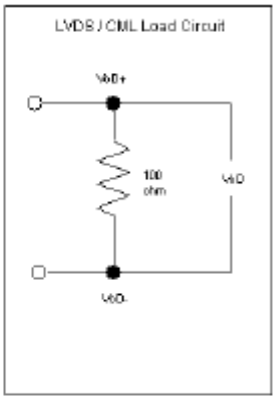
5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/CMOS, TCXO/TCVCXO

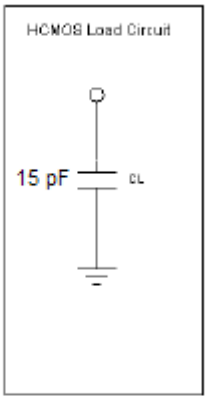
	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions/Notes
Electrical Specifications	Frequency Range	F	50 50		1400 135	MHz MHz	LVPECL, LVDS, CML (Note 4) CMOS
	Operating Temperature	T_A	See Ordering Information			ºC	
	Storage Temperature	T_{STG}	-55		+125	ºC	
	Frequency Stability		See Ordering Information			ppm	(Fmax - Fmin)/2 See Note 1
	Frequency Tolerance at +25ºC		-1.0		+1.0	ppm	
	Frequency Vs. Aging		-3.0 -1.0		+ 3.0 + 1.0	ppm ppm	1st year Per year thereafter.
	Frequency Vs. Supply Voltage			± 0.4		ppm	5% voltage variation
	Frequency Vs. Reflow			± 0.75		ppm	2 reflows max.
	Frequency Vs. Load			± 0.2		ppm	5% supply voltage variation
	Operating Voltage	$V_{cc}/V_s/V_{dd}$	3.135 2.375 1.71	3.3 2.5 1.8	3.465 2.625 1.89	V V V	M6300 M6301 M6302
	Operating Current	I_{CC}			125 100 110 90	mA mA mA mA	LVPECL LVDS CML CMOS
	Rise/Fall Time	Tr/Tf			0.35 6	ns ns	PECL, LVPECL, LVDS CMOS
	Logic "1" Level	V_{OH}	V_{CC}-1.02 90% V_{dd}			V V	LVPECL CMOS
	Logic "0" Level	V_{OL}			V_{CC}-1.63 10% V_{dd}	V V	LVPECL CMOS
	Common Mode Output Voltage	Vcm		1.2		V	LVDS
	Symmetry (Duty Cycle)		45 45 45		55 55 55	% % %	@ 50% Vdd (CMOS) @ 50% of waveform (LVPECL) @ 1.25 V (LVDS)
	Output Voltage Level		0.7	0.95	1.2	Vp-p	CML
	Tuning Range		± 5			ppm	VCTCXO only. See Note 2.
	Voltage Control Range		0.3	1.35	3.0	V	VCTCXO. Pad 2 only.
	Output Skew			20 15 20		ps ps ps	LVPECL CML LVDS
	Output Load		50 Ω to (V_{CC}-2) VDC 100 Ω Differential 15			 pF	See Note 3 LVPECL LVDS, CML CMOS
	Enable/Disable Function		80% 80%		 0.5 0.5	 V V	Outputs enabled (Option B or G) Outputs disabled Outputs enabled (Option S or M) Outputs disabled
	Phase Noise (Typical)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier
	@ 622.080 MHz (LVPECL)	-60	-90	-120	-127	-133	dBc/Hz
	@ 100.000 MHz (HCMOS)	-73	-97	-123	-131	-136	dBc/Hz
	@ 50.000 MHZ (HCMOS)	-80	-102	-130	-137	-141	dBc/Hz
Environmental							
	Shock	Per MIL-STD-202, Method 213, Condition C					
	Vibration	Per MIL-STD-202, Methods 201 & 204					
	Solderability	Per EIAJ-STD-002					
	Hermeticity	1 X 10^{-8} atm cc/sec of helium (Crystal only)					
	Thermal Shock	Per MIL-STD-883, Method 1011, Condition A					
	Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B					

Note 1: Contact factory for less than ± 1ppm frequency stability.
Note 2: Contact factory for other Tuning Range options.
Note 3: See Load Circuit Diagram in this data sheet.
Note 4: Contact factory for frequencies over 945 MHz.

Load Circuit Diagrams







Lead Free Solder Profile